Amendment to the Specification:

Please replace paragraph [0019] with the following amended paragraph:

A method for fabricating the above MIM capacitor structure according to an illustrative embodiment of the present invention will now be described with reference to the perspective views of FIGS. 2-8 and the flow chart of FIG. 9. Referring initially to step 300 of FIG. 9, a first metal layer 210 is deposited over a substrate 200 as shown in FIG. 2. The substrate 200 may be an inter-metal dielectric layer, which has been patterned with contact vias or damascene metal lines, depending upon the IC technology used. ~~The first metal layer 210 may be formed~~ The first metal layer 210 forms the solid continuous metal plate 110 of the MIM capacitor structure shown in FIG. 1A. The substrate 200 may comprise a semiconductor material, such as silicon, and may be covered by an insulating layer (not shown). The substrate 200 may also include circuits, transistors, and other semiconductor devices (not shown). The first metal layer 210 may comprise one or more layers of metal, such as Ti-TiN-AlCu-TiN or Ti-TaN-Cu, depending upon the integrated circuit technology used. The metal layer 210 may be deposited by processes including, without limitation, PVD (physical vapor deposition), CVD metal or plating. The first metal layer 210 may be deposited to a thickness of approximately 200 to 5,000 angstroms.